

I Claim:

1. An integrated synchronous memory operable at different operating frequencies, comprising:

a register storing a frequency-range information item regarding whether the integrated synchronous memory operates in a first frequency range or in a second frequency range in an application, the second frequency range being lower than the first frequency range; and

a subcircuit having a mode of operation controlled on a basis of the frequency-range information item stored in said register, said register connected to said subcircuit.

2. The integrated synchronous memory according to claim 1, wherein said register is a mode register.

3. The integrated synchronous memory according to claim 1, wherein said subcircuit contains a DLL circuit having a variable delay, the variable delay of said DLL circuit being altered on a basis of the frequency-range information item stored in said register.

4. The integrated synchronous memory according to claim 3, wherein said DLL circuit has a signal path with a delay line, said delay line having parts being able to be connected or

disconnected on a basis of the frequency-range information item stored in said register.

5. The integrated synchronous memory according to claim 3, wherein said DLL circuit contains a signal path having a delay line with a series circuit formed of inverter stages, said inverter stages having a switching speed controlled on a basis of the frequency-range information item stored in said register.

6. The integrated synchronous memory according to claim 5, wherein said inverter stages have current sources with a current driver capability controlled on a basis of the frequency-range information item stored in said register.

7. A memory configuration, comprising:

a memory module having at least one synchronous memory, said synchronous memory containing:

a register storing a frequency-range information item regarding whether said synchronous memory operates in a first frequency range or in a second frequency range in an application, the second frequency range being lower than the first frequency range; and

a subcircuit whose mode of operation can be controlled on a basis of the frequency-range information item stored in said register, said register connected to said subcircuit; and

a controller connected to said memory module and setting said register.

8. The memory configuration according to claim 7, further comprising a programmable read-only memory storing a module information item regarding a cut-off frequency used for operating said memory module in an application, said controller reading the module information item from said programmable read-only memory and sets said register in said synchronous memory with a corresponding frequency-range information item.

9. The memory configuration according to claim 8, wherein said memory module is a DIMM module, said synchronous memory is an SDRAM, and said programmable read-only memory is an SPD register.

10. The memory configuration according to claim 7, wherein said controller, in an energy-saving mode of the memory configuration, writes the frequency-range information item to said register of said synchronous memory to operate said

synchronous memory in the second frequency range in the application.